REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-3 and 5-20 are presently pending in this application, Claims 5-18 having been withdrawn from further consideration by the Examiner, Claims 1 and 19 having been amended by the present amendment.

In the outstanding Office Action, Claims 1-3 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Strandberg et al. (U.S. Patent 6,323,435) in view of Westbrook et al. (U.S. Patent 6,203,967), Tsukada et al. (U.S. Patent 6,809,415) and Cooray (U.S. Patent 6,749,927); and Claim 20 was rejected under 35 U.S.C. §103(a) as being unpatentable over modified board of Strandberg et al. in view of Lykins et al. (U.S. Patent 6,440,641).

Claims 1 and 19 have been amended herein. These amendments are believed to find support in the specification, claims and/or drawings as originally filed, for example, the specification, page 18, line 27, to page 20, line 7, as well as Figure 8, and no new matter is believed to be added thereby. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language.

Before addressing the rejections based on the cited reference, a brief review of Claim 1 as currently amended is believed to be helpful. Claim 1 is directed to a multilayer printed wiring board and recites: "a core substrate having a first surface and a second surface on an opposite side of the first surface; a plurality of first conductive layers formed on the first surface and second surface of the core substrate, respectively; a plurality of interlayer insulation layers formed on the first conductive layers, respectively, and the core substrate; and a plurality of second conductive layers formed on the interlayer insulation layers,

respectively, wherein the plurality of first conductive layers on the core substrate includes a plurality of plane conductor layers formed on the first surface and second surface of the core substrate, respectively, the plurality of plane conductor layers of the first conductive layers includes at least one of a power source conductor and a grounding conductor, the core substrate has a through hole penetrating through the core substrate and connecting the first conductive layers on the first and second surfaces of the core substrate, the plurality of second conductive layers includes a plurality of conductor circuits formed on the interlayer insulation layers, respectively, the first conductive layers have a thickness which is larger than a thickness of the second conductive layers on the interlayer insulation layers, and each of the first conductive layers on the core substrate has a side face which is tapered such that an angle, Θ, formed by a straight line connecting the top end and bottom end of the side face of each of the first conductive layers and a horizontal face of the core substrate satisfies $2.8 < \tan \Theta < 55$."

It is respectfully submitted that none of Strandberg et al., Tsukada et al., Cooray and Lykins et al. teaches or suggests "a plurality of first conductive layers formed on the first surface and second surface of the core substrate, respectively ..., wherein *the plurality of first conductive layers on the core substrate includes a plurality of plane conductor layers* formed on the first surface and second surface of the core substrate, respectively, *the plurality of plane conductor layers of the first conductive layers includes at least one of a power source conductor and a grounding conductor, the core substrate has a through hole penetrating through the core substrate and connecting the first conductive layers on the first and second surfaces of the core substrate ..., the first conductive layers have a thickness which is larger than a thickness of the second conductive layers on the interlayer insulation layers, and each of the first conductive layers on the core substrate has a side face which is tapered such that an angle, Θ, formed by a straight line connecting the top end and bottom end of the side face*

of each of the first conductive layers and a horizontal face of the core substrate satisfies 2.8 < tan Θ < 55" as recited in amended Claim 1 (emphasis added in italic).

More specifically, Strandberg et al. only shows a laminate structure in which a wiring pattern consisted of conductive traces (14a, 14b) is formed on a laminate board (12), not plane conductor layers. Also, it is believed that Strandberg teaches away from making plane conductor layers and the thickness of the conductive layers on the core substrate larger than the thickness of the conductive layers on the interlayer insulation layer. That is, Strandberg et al. emphasizes reduced stress features reducing metallization present on its laminated printed circuit board[1] and states that "the force per unit area exerted on the dielectric material 32 could be reduced by reducing the area of one or more of the sides of the conductive traces 14*a*, 14*b* and conductive [pad] 22*a*,"[2] that these conductive traces (14a, 14b) in Figs. 1-5 have a thickness in the range of 20 μm to 30 μm[3] and that the wiring pattern (114a) on the substrate (112) has a thickness in the range of 10 μm to 20 μm,[4] thus making the conductive pattern on the surface of the substrate much thinner with much less filler to provide a lower dielectric constant to the structure and thus a lower impedance.[5]

Tsukada et al. merely describes providing superior adhesion between a substrate and a conductor pattern by forming a conductor pattern with a trapezoidal cross-section and a solder resist coated on the conductor pattern, Cooray shows a core substrate, wiring layers (8) formed inside the core substrate, fine wiring layers (7) formed on both sides of the core substrate and a through hole (5) connecting the fine wiring layers (7) on both sides of the core substrate, and Westbrook et al. describes providing a grounding plane layer (a patterned conductive layer or a metal clad conductive layer) on the surface of a high density

[1] See Strandberg, column 4, lines 52-67.
[2] See id., column 7, lines 16-29.
[3] See id, column 8, lines 4-9.
[4] See id., column 9, lines 16-23.
[5] See id, column 9, lines 23-34.

interconnect wiring board, *not a core substrate*. Lykins et al. is cited simply for the copper foil and plated films of the first conductive layers.

Thus, Strandberg et al., Tsukada et al., Cooray and Lykins et al. are not believed to teach or suggest conductive layers in which plane conductor layers are formed on the opposing surfaces of a core substrate in such a manner that the plane conductor layers include a power source conductor and/or a grounding conductor, that the core substrate has a through hole connecting the conductive layers on the opposing surfaces of the core substrate, and that the thickness of the conductive layers is larger than the thickness of conductive layers on interlayer insulation layers. Accordingly, the structure recited in Claim 1 is believed to be distinguishable from Strandberg et al., Tsukada et al., Cooray and Lykins et al.

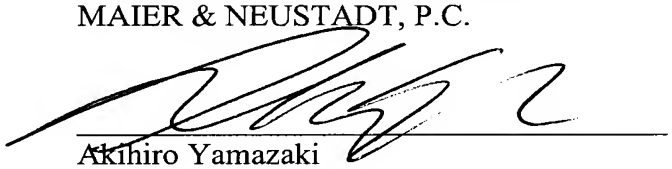
Because none of Strandberg et al., Tsukada et al., Cooray and Lykins et al. discloses the first conductive layer structure as recited in Claim 1, their teachings even in combination are not believed to render the multilayer printed wiring board of Claim 1 obvious.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 2, 3, 19 and 20 depend from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 2, 3, 19 and 20 are believed to be allowable as well.

In view of the amendments presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Akihiro Yamazaki
Attorney of Record
Registration No. 46,155

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/07)